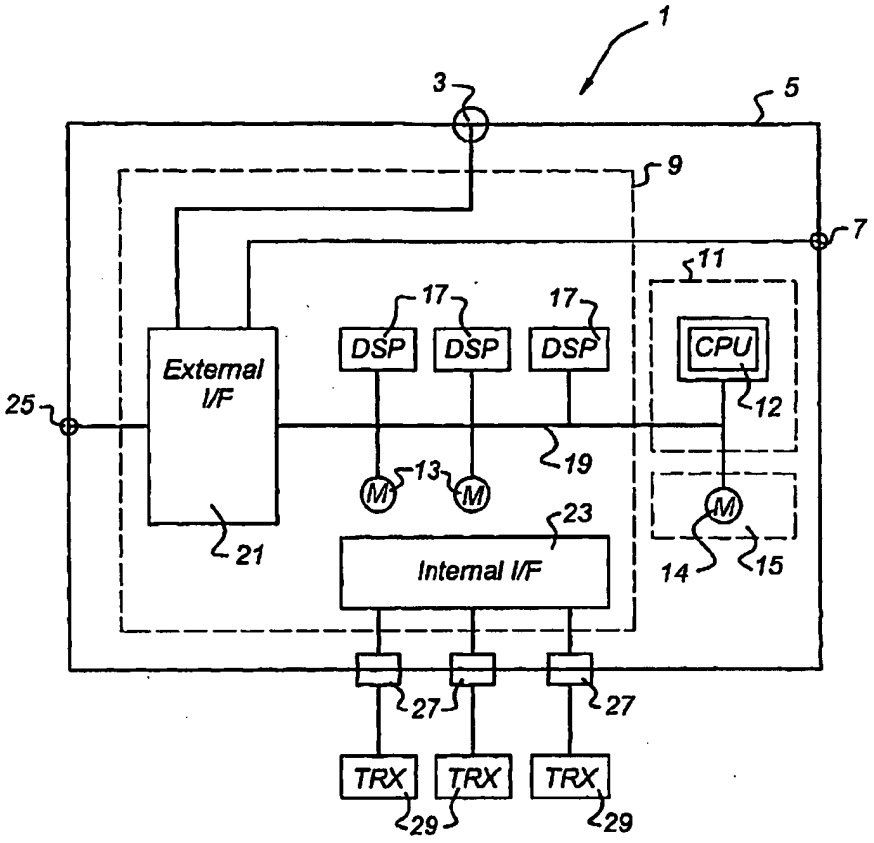
Fig 1 Prior art



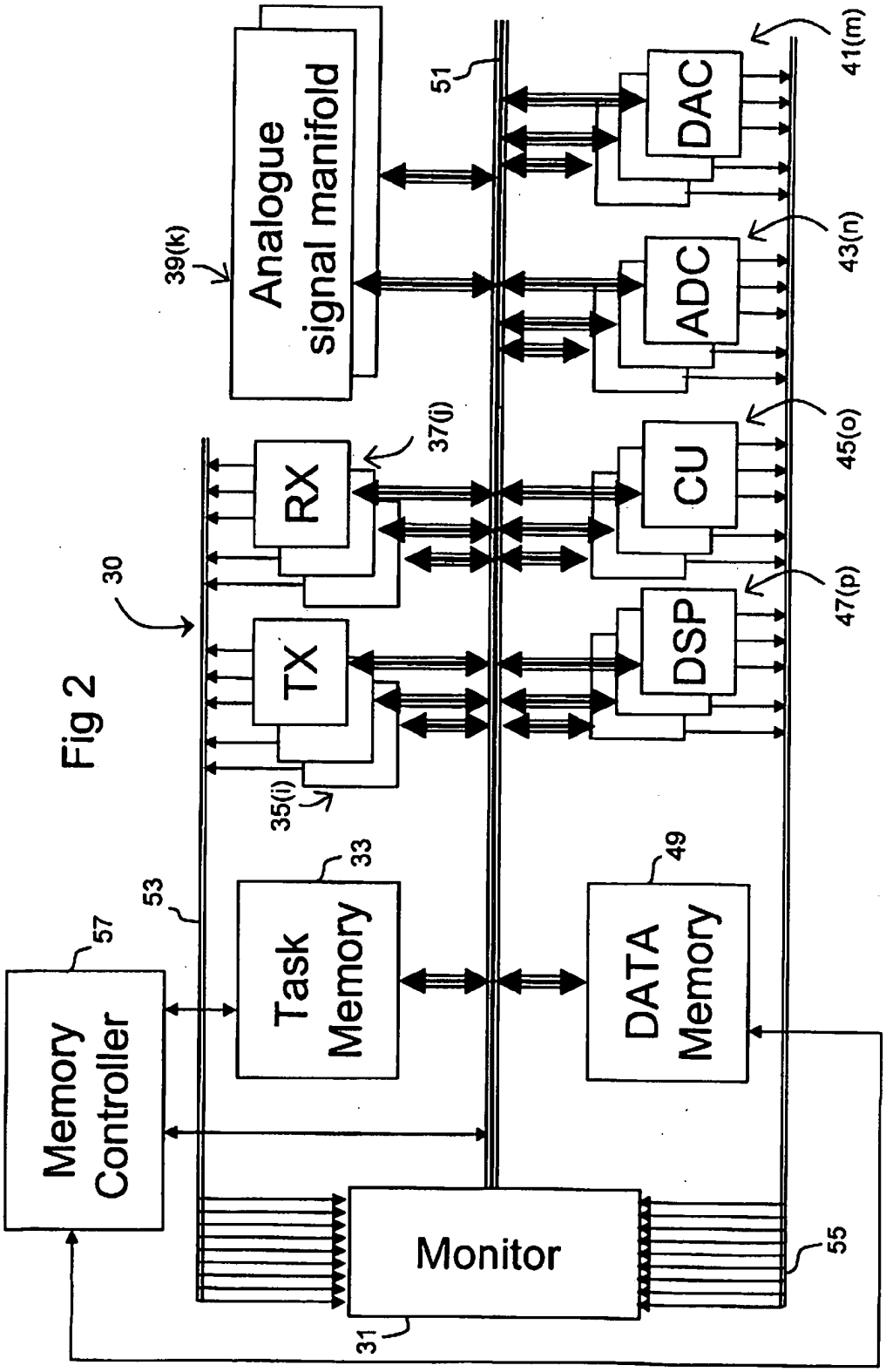

Analogue signal manifold
39(k)
51
DAC
41(m)
ADC
43(n)
CU
45(o)
DSP
47(p)
RX
37(j)
TX
35(j)
30
Task Memory
33
DATA Memory
49
Memory Controller
57
53
Monitor
31
55

Fig 2

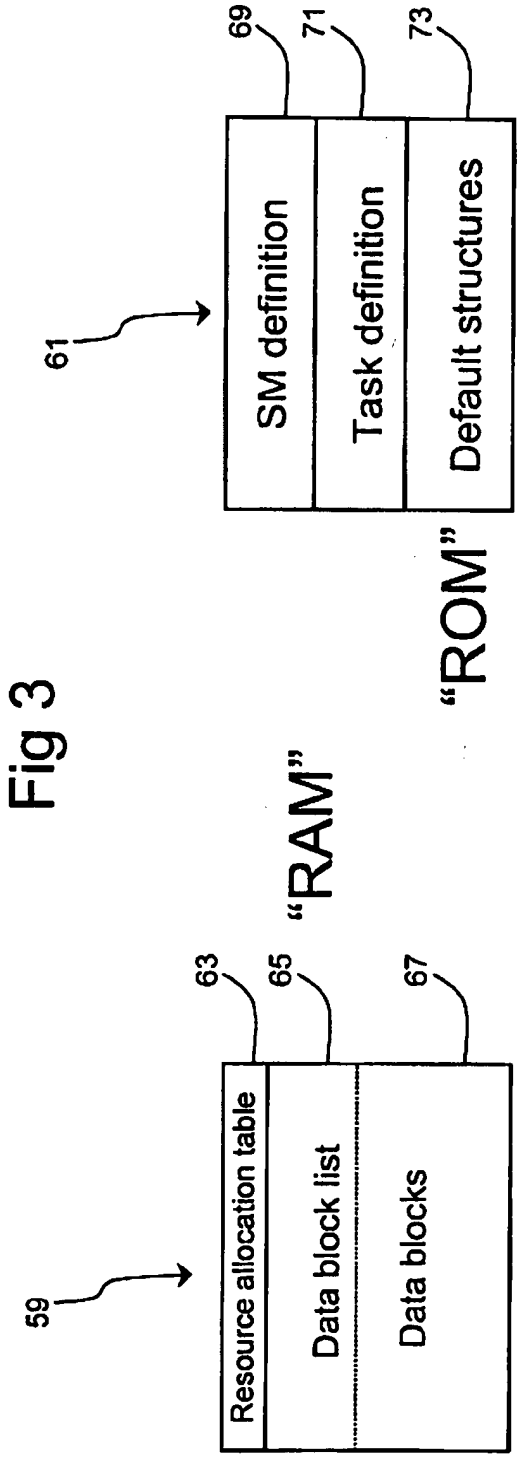

61
69
71
73
SM definition
Task definition
Default structures
"ROM"
"RAM"
59
63
65
67
Resource allocation table
Data block list
Data blocks

Fig 3

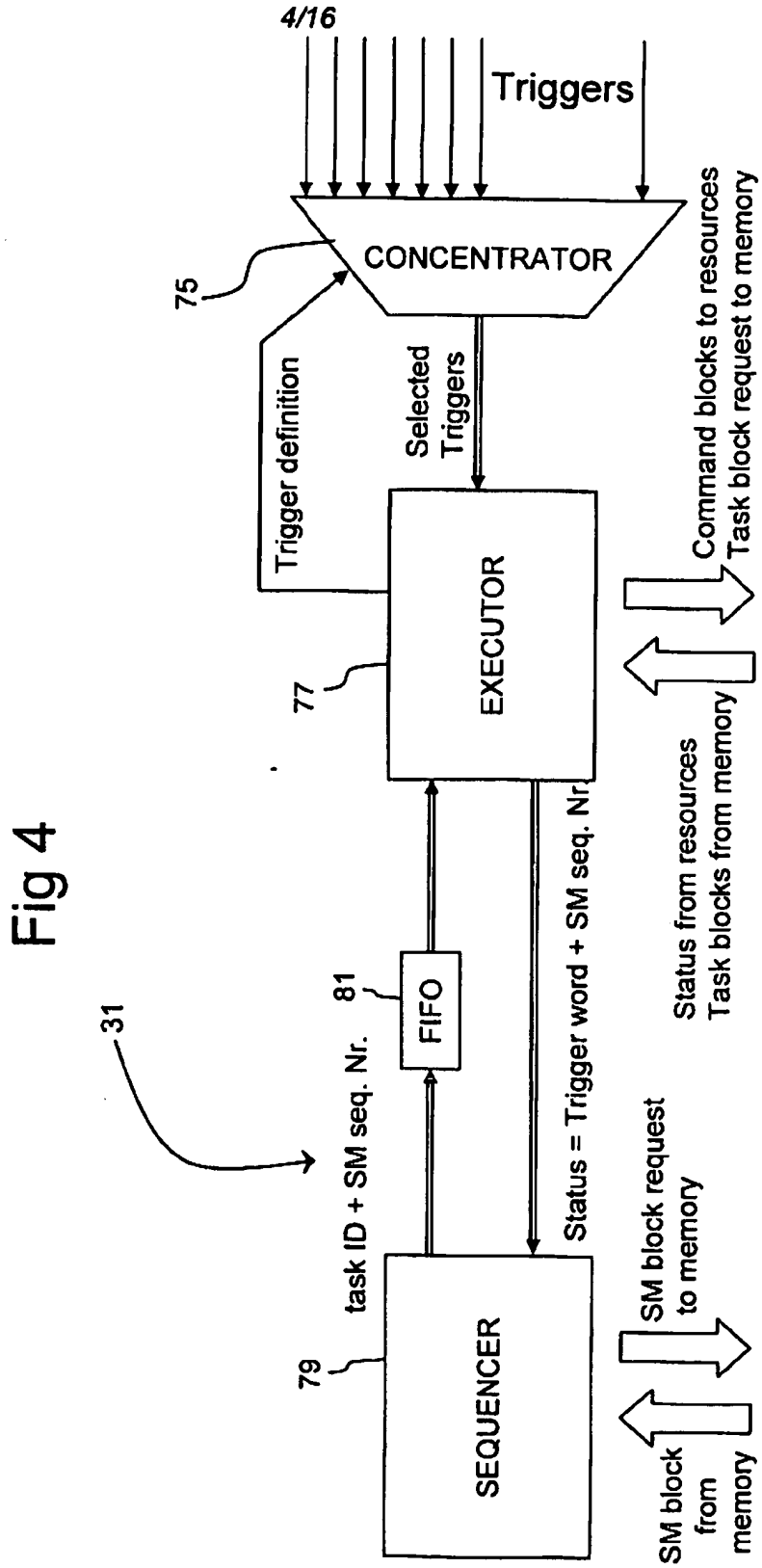

Triggers
CONCENTRATOR
75
Trigger definition
Selected Triggers
EXECUTOR
77
Command blocks to resources
Task block request to memory
Status from resources
Task blocks from memory
31
81
FIFO
task ID + SM seq. Nr.
Status = Trigger word + SM seq. Nr.
SEQUENCER
79
SM block request to memory
SM block from memory

Fig 4

Fig 5

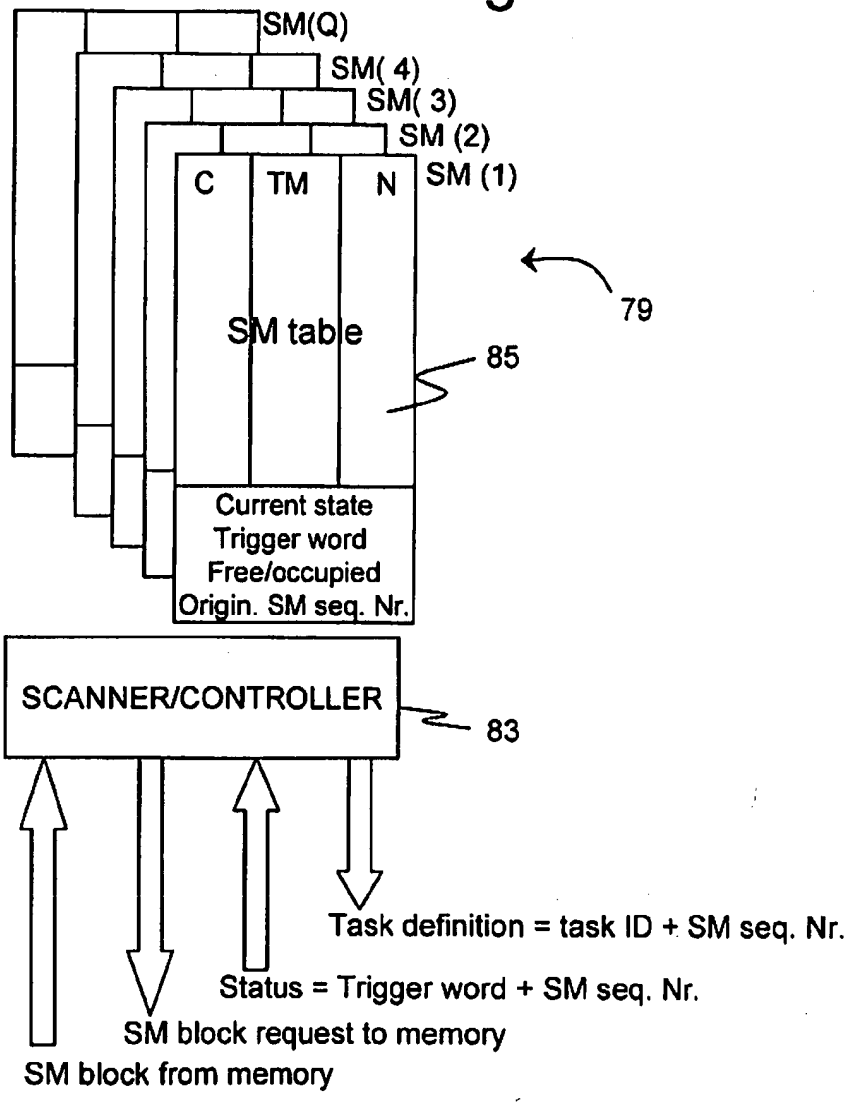

SM(Q)
SM(4)
SM(3)
SM (2)
SM (1)
C
TM
N
79
SM table
85
Current state
Trigger word
Free/occupied
Origin. SM seq. Nr.
SCANNER/CONTROLLER
83
Task definition = task ID + SM seq. Nr.
Status = Trigger word + SM seq. Nr.
SM block request to memory
SM block from memory

Fig 6

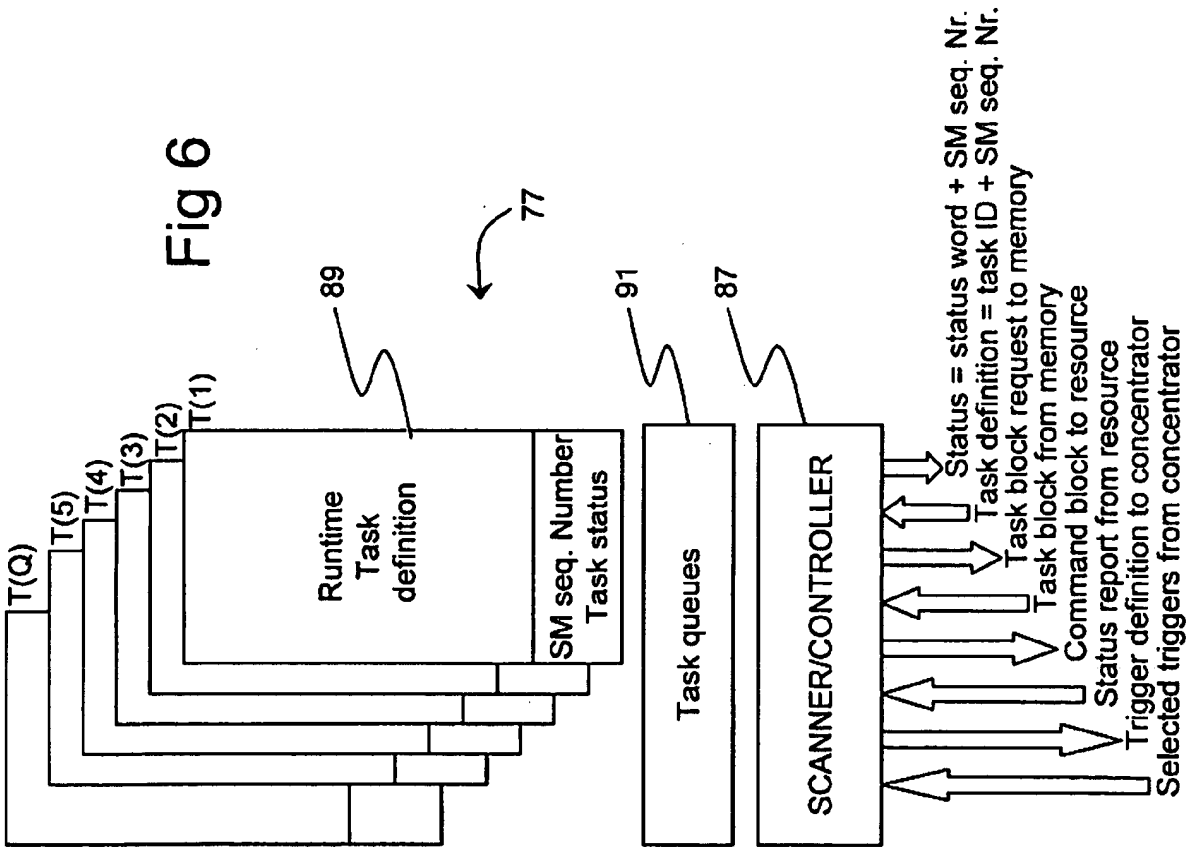

T(Q)
T(5)
T(4)
T(3)
T(2)
T(1)
Runtime Task definition
SM seq. Number Task status
89
77
91
87
Task queues
SCANNER/CONTROLLER
Status = status word + SM seq. Nr.
Task definition = task ID + SM seq. Nr.
Task block request to memory
Task block from memory
Command block to resource
Status report from resource
Trigger definition to concentrator
Selected triggers from concentrator

Fig 7

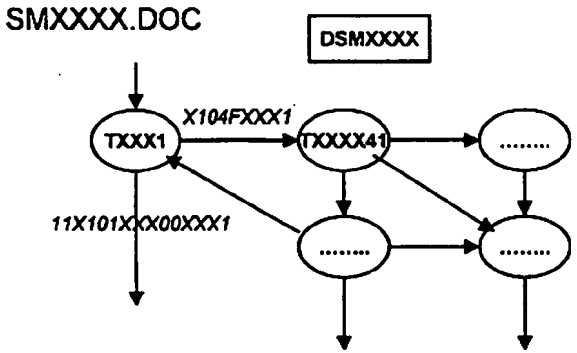
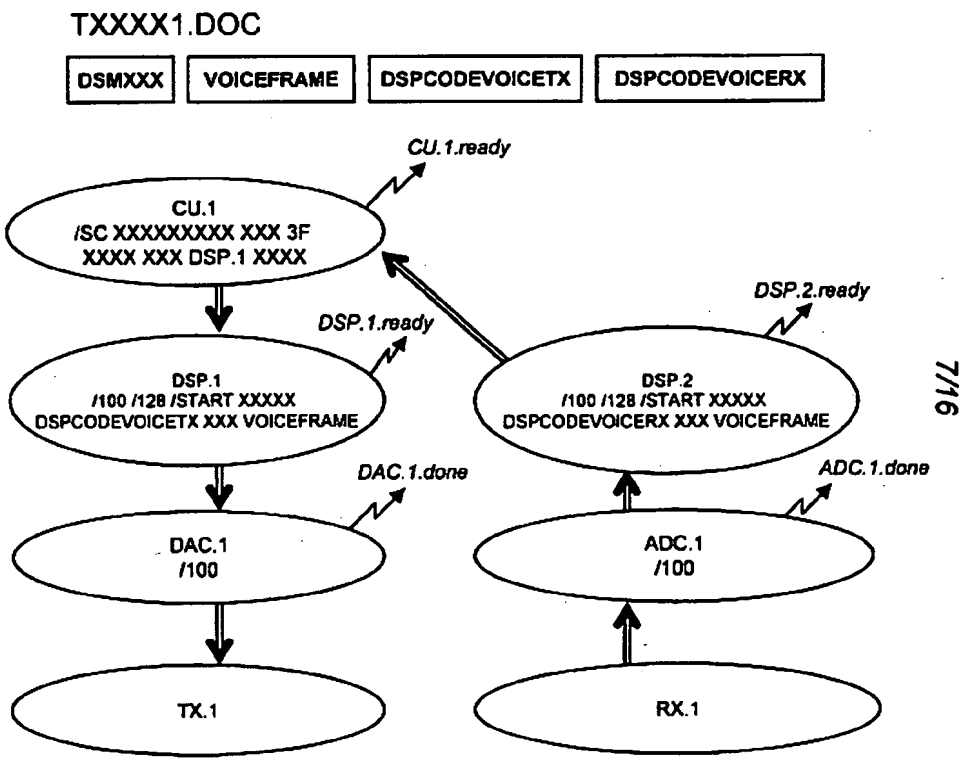


Fig 8



TASK-TRIGGER WORD:
1A,0,0,1,ADC.1.done,DAC.1.done,DSP.1.ready,DSP.2.ready,CU.1.ready,
DSP.1.status,DSP.2.status

REPLACEMENT SHEET

7/16

Fig 9

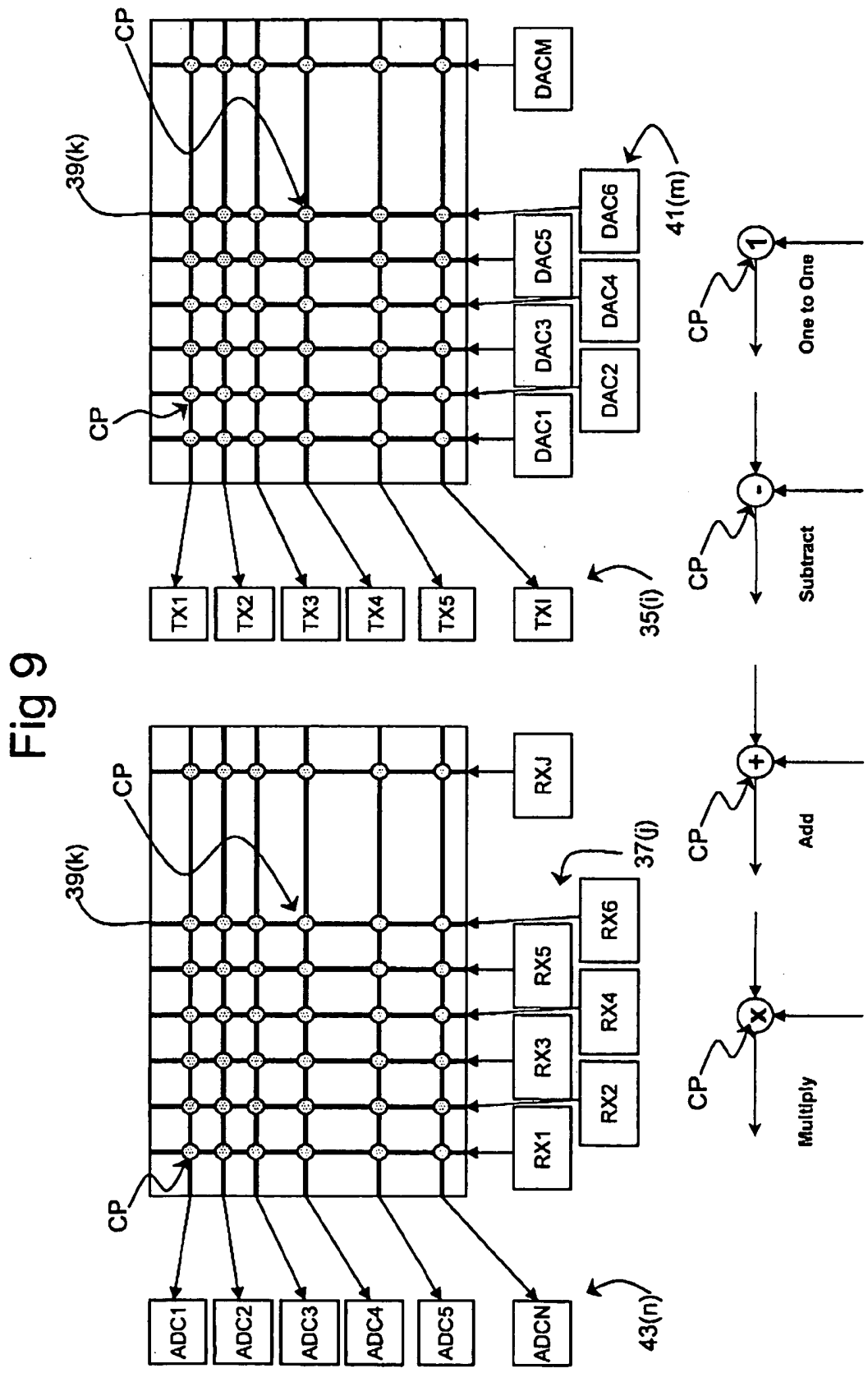
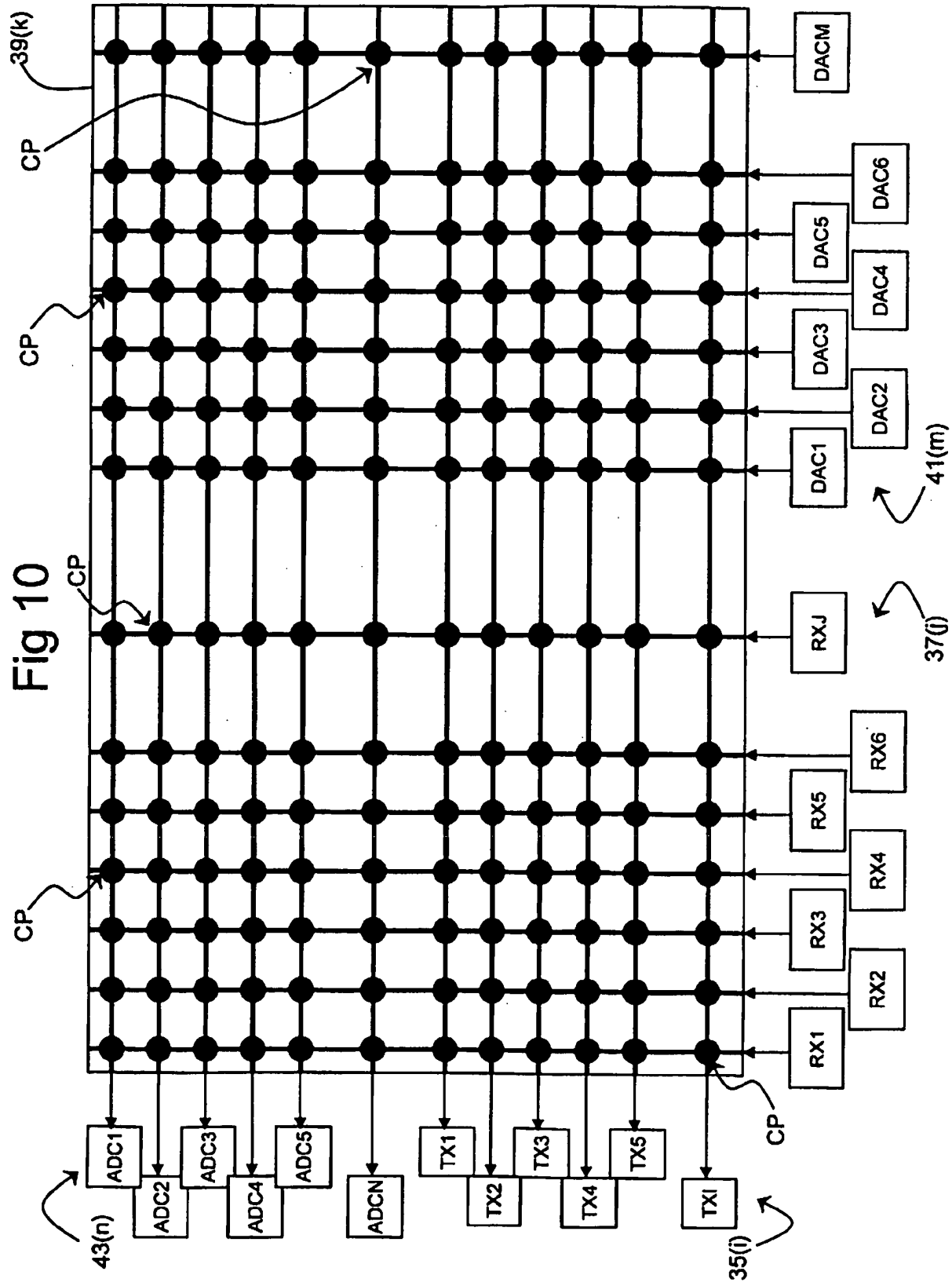

CP
39(k)
DACM
41(m)
DAC6
DAC5
DAC4
DAC3
DAC2
DAC1
TX1
TX2
TX3
TX4
TX5
TXI
35(i)
RXJ
37(j)
RX6
RX5
RX4
RX3
RX2
RX1
ADC1
ADC2
ADC3
ADC4
ADC5
ADCN
43(n)
One to One
Subtract
Add
Multiply

Fig 10


39(k)
CP
CP
CP
CP
DACM
DAC6
DAC5
DAC4
DAC3
DAC2
DAC1
41(m)
RXJ
37(j)
RX6
RX5
RX4
RX3
RX2
RX1
CP
ADC1
ADC2
ADC3
ADC4
ADC5
ADCN
TX1
TX2
TX3
TX4
TX5
TXI
43(n)
35(i)

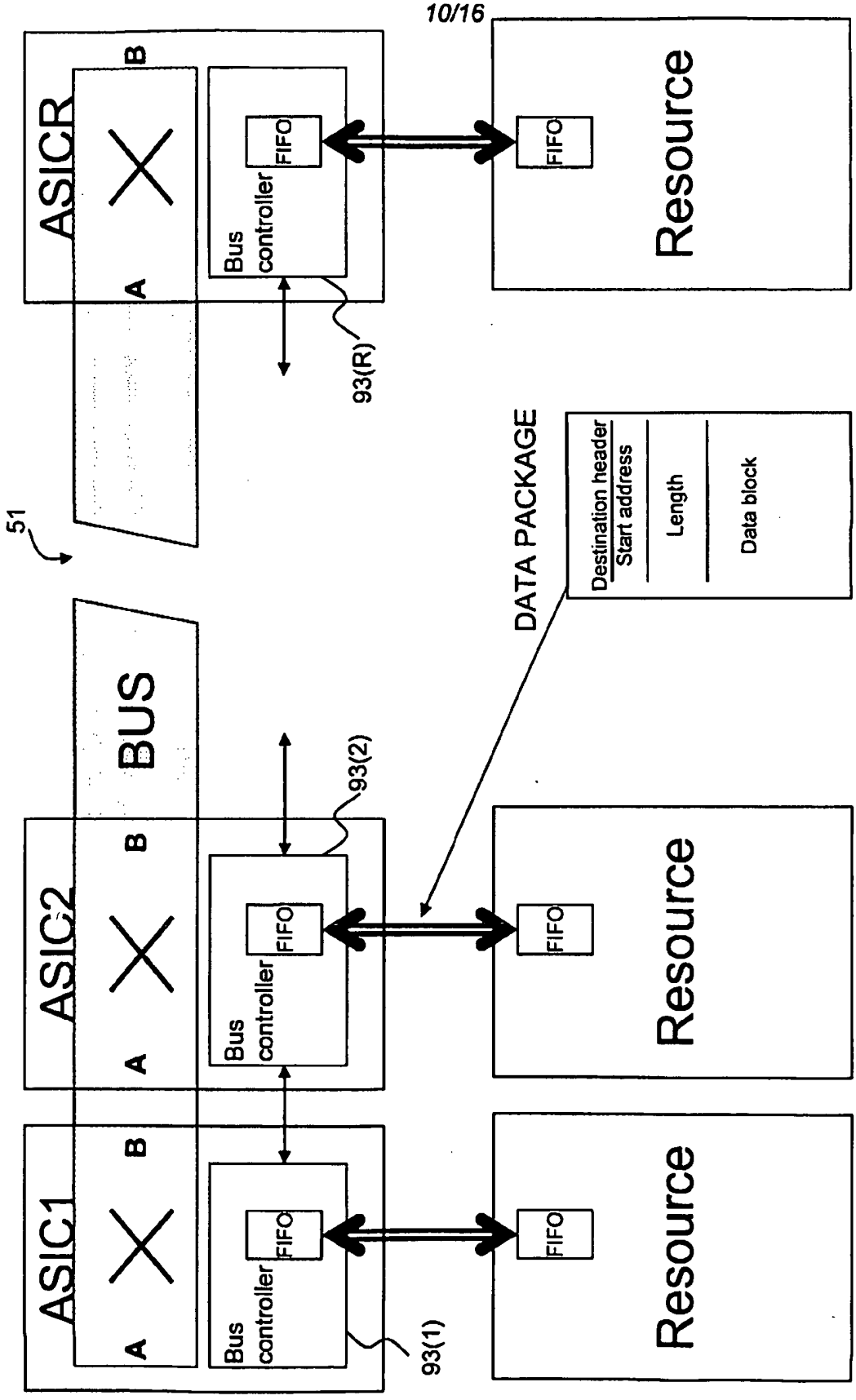

ASICR
A
B
Bus controller
FIFO
93(R)
Resource
51
BUS
ASIC2
93(2)
ASIC1
93(1)
DATA PACKAGE
Destination header
Start address
Length
Data block

Fig 11

Fig 12

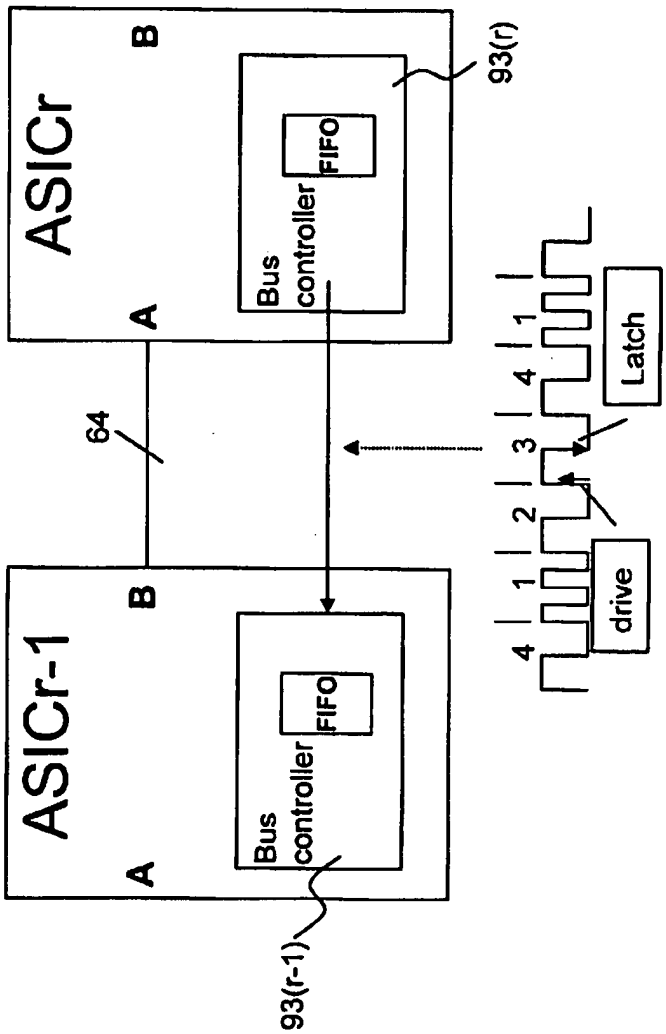

ASICr
B
A
Bus controller
FIFO
93(r)
64
ASICr-1
B
A
Bus controller
FIFO
93(r-1)
1
2
3
4
Latch
drive

Fig 13

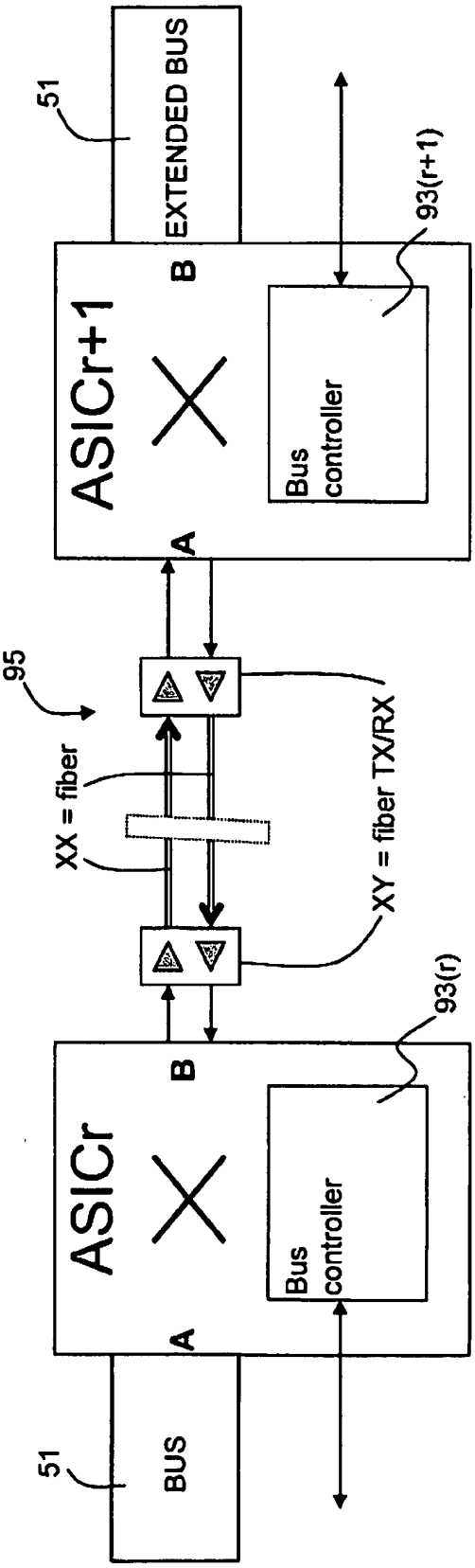

51
EXTENDED BUS
93(r+1)
B
ASICr+1
Bus controller
A
95
XX = fiber
XY = fiber TX/RX
93(r)
B
ASICr
Bus controller
A
51
BUS

Fig 14

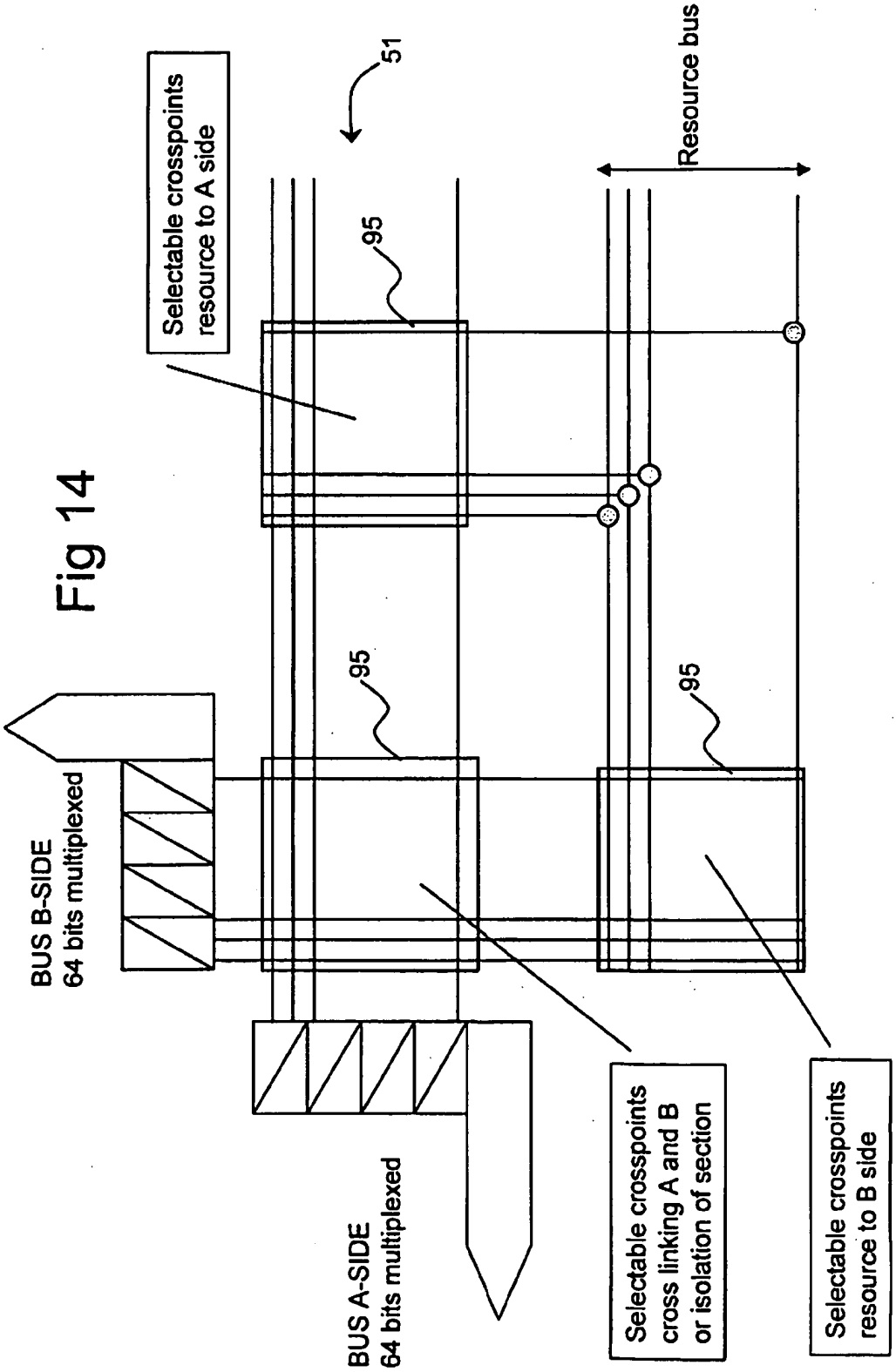

Selectable crosspoints resource to A side
51
Resource bus
95
95
95
BUS B-SIDE
64 bits multiplexed
BUS A-SIDE
64 bits multiplexed
Selectable crosspoints cross linking A and B or isolation of section
Selectable crosspoints resource to B side

Fig 15

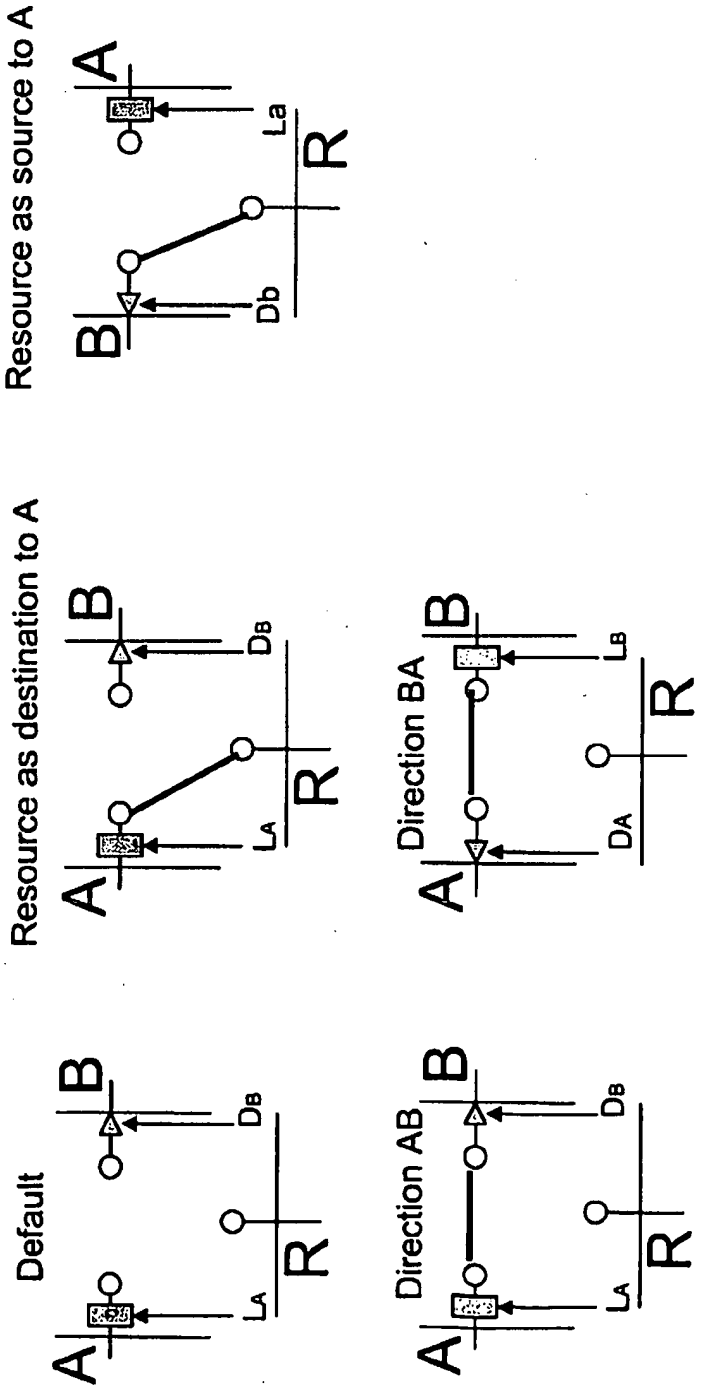

Default
A
B
R
LA
DB
Resource as destination to A
A
B
R
LA
DB
Direction AB
A
B
R
LA
DB
Resource as source to A
A
B
R
La
Db
Direction BA
A
B
R
DA
LB

Fig 16a

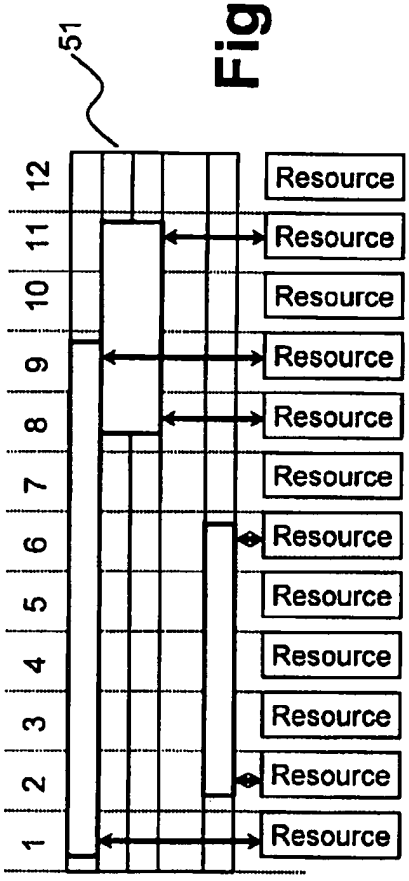


Fig 16b

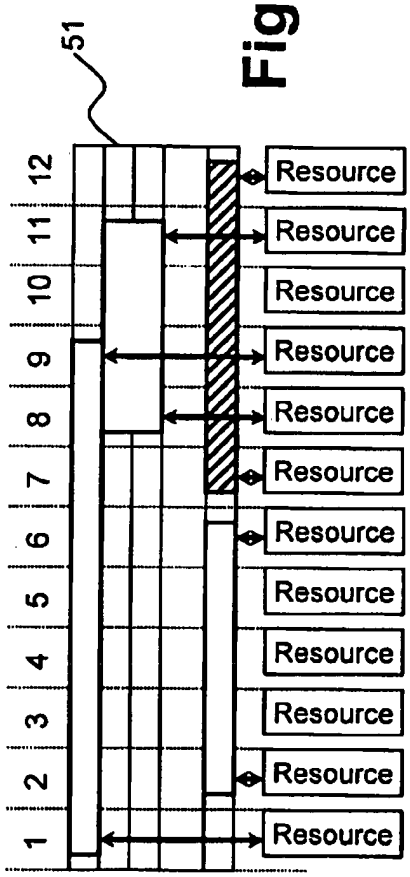


Fig 16c

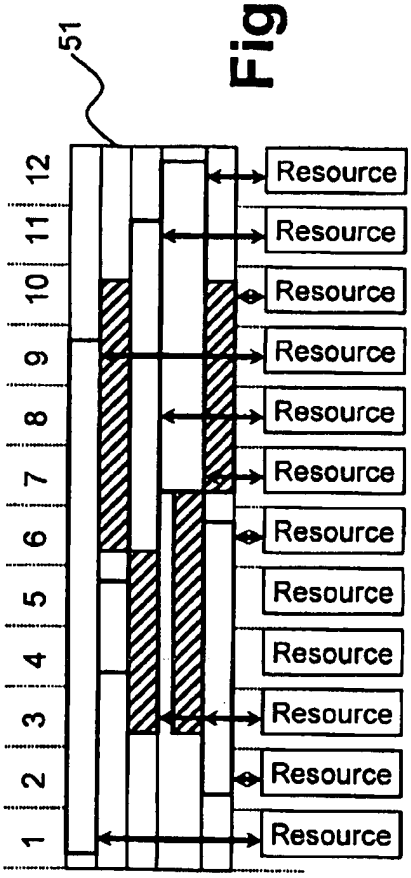
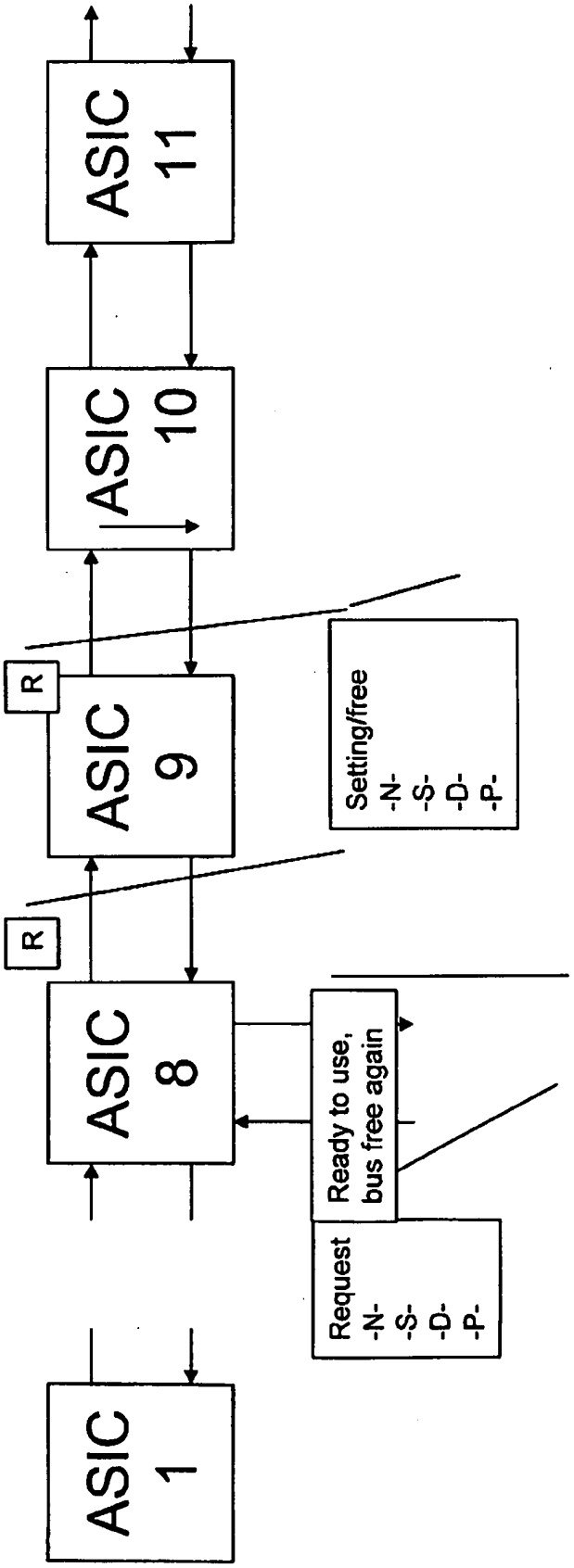


Fig 17


ASIC 11
ASIC 10
R
ASIC 9
Setting/free
-N-
-S-
-D-
-P-
R
ASIC 8
Ready to use, bus free again
Request
-N-
-S-
-D-
-P-
ASIC 1